APPLICATION FOR UNITED STATES LETTERS PATENT

LOW DEVIATION INDEX DEMODULATION SCHEME

Inventors:

JONATHON CHEAH
JIANPING PAN
LE LUONG

Prepared by:

Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8598

Attorney Docket No. 04939P011

"Express Mail" mailing label number EL143569485US
Date of Deposit December 20, 2001
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Patricia A. Balero
(Typed or printed name of person mailing paper or fee)

[signature]
(Signature of person mailing paper or fee)

LOW DEVIATION INDEX DEMODULATION SCHEME

FIELD OF THE INVENTION

[0001] The present invention relates to a demodulation solution for a wireless transceiver that operates in a low deviation index transmission protocol environment, for example a Bluetooth-compatible wireless transceiver.

BACKGROUND

[0002] Bluetooth wireless technology is an emerging communication solution that allows users to make wireless and instant connections between various communication devices, such as mobile phones and desktop and notebook computers. Because Bluetooth uses radio transmissions, transfer of both voice and data can occur in real time. This sophisticated mode of transmission adopted in the Bluetooth specification ensures protection from interference and security of data.

[0003] The Bluetooth radio is designed to operate in a globally available frequency band, ensuring communication compatibility worldwide. The Bluetooth specification has two power levels defined; a lower power level that covers a personal area within a room, and a higher power level that can cover a larger area, such as a home. Software controls an identity coding built into each radio to ensure that only those units preset by their owners can communicate with one another.

[0004] Bluetooth wireless technologies support both point-to-point and point-to-multipoint connections. With the current specification, up to seven

"slave" devices can be set to communicate with a "master" radio in one device. Several of these so-called "piconets" can be established and linked together in ad hoc "scatternets" to allow communication among continually flexible configurations. All devices in the same piconet have priority synchronization, but other devices can be set to enter at any time. This topology can best be described as a flexible, multiple piconet structure.

[0005] Although Bluetooth presents an extremely flexible and desirable communication architecture for computer vendors and vendors of other personal digital assistants and the like, there are several challenges associated with implementing Bluetooth-compatible devices. For example, the specifications governing the implementations of Bluetooth-compatible transmitters and receivers (see, Specification of the Bluetooth System, vol. 1.0b, December 1, 1999, published by Bluetooth Special Interest Group and available via the World Wide Web at www.bluetooth.com) indicate that such devices must be capable of operating using Gaussian Frequency Shift Keying (GFSK) with a BT product of approximately 0.5 and a deviation index or modulation index (h) of approximately 0.32. In this scheme, a binary "1" is represented by a positive frequency deviation (from the carrier frequency) and a binary "0" is represented by a negative frequency deviation.

[0006] The "BT" product is the product (i.e., a mathematical multiplication operation) of the occupied bandwidth of a communication signal and the bit period thereof. It is used by engineers and others in the relevant art as a shorthand expression for communicating information regarding the effective band limiting of a transmitted signal. With Bluetooth, the bit period (T), which is

an indication of the keying rate, is specified as 1 MHz. Thus, the available bandwidth for a transmitted signal to occupy (B) is 0.5 MHz.

[0007] The deviation index (h) is a measure of the difference in frequency for an FSK modulation scheme (as is used by Bluetooth radios) between different bits. That is, the difference in the modulation frequency for transmission of a logical "1" versus a logical "0". Since the modulation frequency (or keying rate) is specified as 1 MHz and h = 0.32, this gives a maximum deviation frequency f_D = (0.32 x 1) / 2 MHz = 160 kHz.

[0008] This small deviation index presents a problem. One cycle of a 160 kHz sine wave has a period of approximately 6.25 µsec. But the keying rate in Bluetooth is 1 MHz (i.e., a period of 1 µsec), so that even before a complete cycle of a bit can be modulated onto the carrier during transmission, the time for transmitting the next bit has already arrived. Thus, at most only approximately one sixth of a cycle of the data signal will be available at the receiver for decoding. For this reason a decoding solution for a low deviation index transmission scheme is needed.

SUMMARY OF INVENTION

[0009] In one embodiment, a wireless receiver, e.g., a Bluetooth-compatible receiver or a receive chain in a Bluetooth-compatible transceiver, includes a discriminator unit and a timing recovery unit. The output of the discriminator unit is provided as an input to the timing recovery unit, which timing recovery unit is configured to align a free-running clock of the receiver with a received signal to extract received data therefrom.

[0010] These and other embodiments of the present invention are more fully described below and illustrated in the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings in which:

[0012] **FIG. 1** illustrates a conventional radio receiver architecture;

[0013] **FIG. 2** illustrates a radio receiver architecture configured in accordance with one embodiment of the present invention;

[0014] **FIG. 3** illustrates one example of a demodulator for use in the radio receiver architecture shown in **FIG. 2** in further detail;

[0015] **FIG. 4** illustrates one example of a discriminator, which is a digital differential detector in particular, for use in the demodulator shown in **FIG. 3** in further detail;

[0016] **FIG. 5** illustrates one example of an implementation of a low pass filter for use in the discriminator shown in **FIG. 3** in further detail;

[0017] **FIG. 6** is a waveform diagram illustrating an example of an output signal from the one-bit analog to digital converter of the discriminator shown in **FIG. 4**;

[0018] **FIGS. 7 and 8** are waveform diagrams illustrating examples of output signals from the inverter of exclusive OR (XORNOT) operations performed in the discriminator shown in **FIG. 4**;

[0019] **FIGS. 9 and 10** are waveform diagrams illustrating examples of output signals from the shift registers of the discriminator shown in **FIG. 5**;

[0020] **FIG. 11** is a waveform diagram illustrating an example of an output signal from the adder of the discriminator shown in **FIG. 5**;

[0021] FIG. 12 is a waveform diagram illustrating an example of an output signal from the detector of the discriminator shown in FIG. 5;

[0022] FIG. 13 is a waveform diagram illustrating an example of an output signal from the edge detector of a timing recovery unit shown in FIG. 16B;

[0023] FIG. 14 is a waveform diagram illustrating an example of an output signal from the divide-by 24 unit of the timing recovery unit shown in FIG. 16B;

[0024] FIG. 15 is an example of an edge detector for the timing recovery unit shown in FIG. 16B;

[0025] FIG. 16A is an example of a timing recovery unit;

[0026] FIG. 16B is a more detailed view of the timing recovery unit shown in FIG. 16A;

[0027] FIG. 16C is a diagram illustrating alignment of a clock signal with a data signal;

[0028] FIG. 16D is a diagram illustrating non-alignment of a clock signal with a data signal; and

[0029] FIG. 17 is a waveform diagram illustrating an example of an output signal from the demodulator shown in FIG. 2.

DETAILED DESCRIPTION

[0030] Described herein is a demodulation solution for use with transceivers and/or receivers that operate in low deviation index environments, such a Bluetooth-compatible transceivers and receivers. Although the present invention is discussed with reference to certain illustrated embodiments thereof, it should be kept in mind that this discussion and the accompanying illustrations are merely examples of the broader spirit and scope of the present invention. These examples and the accompanying illustrations are provided in order to communicate the nature of the present invention; however, the present invention itself is best understood with reference to the claims, which follow this detailed description.

[0031] In addition to providing a solution for low deviation index environments, the present demodulation solution provides a solution for a system-on-a-chip implementation of a wireless transceiver or receiver. By system-on-a-chip it is meant that virtually the entire transceiver or receiver will be fabricated on a single semiconductor die. To make such implementations viable, it is important to keep the number of external components to a minimum. Such external components, often active components such as capacitors, inductors and the like, are often needed because semiconductor fabrication processes are not appropriate for creating these components and/or such fabrication is cost-prohibitive. With conventional receivers (or receive chains in a transceiver), such as the receiver 10 shown in **FIG. 1**, there is often a need for several external components.

[0032] In receiver 10, signals from antenna 12 are first amplified by a low noise amplifier (LNA) 14 and then down-converted by mixer 16 using a local oscillator 18. The resulting intermediate frequency (IF) signal may then be filtered using one or more stages of band-pass filtering in so-called IF amplifiers/filters, such as IF filter 20. Ultimately, the received signal is passed to a demodulator 22 for extraction of the received data, which is presented as an output of the demodulator 22. The various filters and local oscillators of receiver 10 may have several active components associated therewith and, particularly in the case of such filters, these components may be physically large in order to provide the necessary noise immunity and attenuation of unwanted signal components. Thus, such an implementation is not well suited for implementation as a system-on-a-chip.

[0033] Therefore, rather than adopting the traditional implementation, a receiver (or receive chain for a transceiver) having a different architecture may be used in a system-on-a-chip implementation. One example of such a receiver (or receive chain) is illustrated in **FIG. 2**. In receiver 24, signals from antenna 26 are first amplified by low noise amplifier 28 and then passed to a poly-phase network 30. Poly-phase complex filter 36 may be composed of a high-quality band-pass filter and a sampling rate converter which brings the sampling frequency down to the required one for the given application; i.e., the front-end of receiver 24, to perform the direct conversion to digital at the radio frequency (RF). The outputs of poly-phase network 30 are the in-phase (I) and quadrature (Q) signal components of the RF signal, which components are each down-converted to an IF signal using mixers 32 and local oscillator 34. The resulting

IF signals (which in one embodiment are at an IF of approximately 2 MHz) are then applied to a complex filter 36.

[0034] Complex filter 36 eliminates the imaginary components of the IF signals and the resulting output signals 38A and 38B are applied as inputs to a demodulator 40. Demodulator 40 extracts the original data signal from the input IF signals and provides output data 42. As will be discussed below, the demodulator 40 may be regarded as a discriminator and timing recovery unit.

[0035] By adopting the above-described architecture, receiver (or receive chain if it is used as part of a transceiver) 24 may be synthesized on a single integrated circuit. The use of the poly-phase network 30 and complex filter 36 eliminates the bulky active and passive components that would otherwise be required in a conventional receiver architecture, thereby allowing for system-on-a-chip implementation.

[0036] Note that the above-described embodiment of receiver 24 may be regarded as a "low-IF" receiver. That is, it is a receiver having an IF less than the tuning bandwidth. Conventional radio receivers usually have an intermediate frequency greater than the tuning bandwidth to ensure that all channels within that tuning bandwidth are passed by the IF filters. In the case of a Bluetooth radio, the transmission spectrum is between 2.4 GHz and 2.4835 GHz, thus leaving a pass-band (or tuning bandwidth) of 83.5 MHz. Conventional Bluetooth radios often employ an IF of approximately 110 MHz; greater than the tuning bandwidth. However, in the present receiver architecture an IF of only 2 MHz is used. Indeed, if one desires this IF can be eliminated and brought to base-band, however, the 2 MHz (or similar intermediate frequency) is preferred in order to

keep the size of various active components (e.g., capacitors) more manageable under today's component fabrication process limitations.

[0037] Having thus described the overall receiver architecture, the particulars of the demodulation scheme may now be discussed. **FIG. 3** illustrates demodulator 40 in more detail. As shown, demodulator 40 includes a discriminator 44 and a timing recovery unit 46. The discriminator 44 is used to extract the over-sampled data from the input signals 38a and 38b. The timing recovery unit 46 then aligns a 1 MHz clock signal (produced from a local 24 MHz free-running clock) with the rising edge of the data signal and this bit-timing clock 48 is used to extract the output data 42 from the over-sampled data signal 52.

[0038] Portions of discriminator 44 are shown in greater detail in **FIG. 4**. For this diagram, only one signal path is shown, however, it should be appreciated that a signal path such as that shown in the drawing is used for both signals 38A and 38B from the complex filter 36. For this reason, a single input signal 38 is illustrated and the use of this reference number is meant to indicate that the path is similar for both signals 38a and 38b.

[0039] The signal 38 from complex filter 36 is provided as the input to a one-bit analog to digital (A/D) converter (also known as a bit-slice unit or zero crossing detector) 54. The output 56 of the one-bit A/D converter 54 is logically XORNOTed with a delayed replica of itself in what is essentially a multiplication process 58. The resulting signal 62 is low pass filtered 64 to produce output signal 52. The delay 60 is set as:

$$T_{delay} = [(2n+1)\pi] / 2\omega_0 = (2n+1) / 4f_0, \quad \textbf{(1)}$$

where f_0 is the intermediate frequency (IF). If T_b represents one bit period, then the data rate $f_b = 1 / T_b$. Want $T_{delay} < T_b$, substitution in equation **(1)**, yields:

$$(2n+1) / 4f_0 < T_b \qquad \textbf{(2)}$$

Further substituting $T_b = 1/ f_b$ in equation (2), yields:

$$2n+1 < 4f_0 / f_b \qquad \textbf{(3)}$$

Thus, the detector must have the largest integer n that satisfies equation **(3)**.

In an embodiment where the intermediate frequency f_0 is 2.0 Mhz and the data rate f_b is 1 Mbps, n = 3.0.

[0040] One implementation of the low pass filter 64 is shown in **FIG. 5**. In this illustration, both the I and Q signal paths are shown from the point of the XORNOT operation 58 forward. The signals 62A and 62B (using the notation conventions discussed above) are each supplied as inputs to respective 48-bit shift registers 64A and 64B. The shift registers 64A and 64B are clocked at 48 MHz using the same local clock discussed above and the outputs 66A and 66B of the shift registers are applied to a 7-bit adder 68. The adder is used as an accumulator and its output signal 70 is applied as an input to detector 72. The output of detector 72 is signal 52, which is a logic "1" for a condition where the sum of the outputs of the shift registers 66A and 66B is greater than 47 and is a logic "0" when this sum is less than or equal to 47.

[0041] At this point it is helpful to review examples of the waveforms that might actually be present at various points in demodulator 40. **FIG. 6** illustrates the output of the one-bit A/D converter 54. Note that this signal will be present in both the I and Q signal paths as discussed above. By examining the waveform

shown in this diagram, one can see the presence of the frequency modulated data superimposed on the carrier at the 1 MHz bit rate.

[0042] **FIG. 7** illustrates the output signal 62A from the XORNOT operation 58a. Again similar signals would be present in both the I and Q signal paths, and the corresponding signal 62B is shown in **FIG. 8**. **FIGS. 9 and 10** illustrate the waveforms for signals 66A and 66B, respectively. Note that the outputs of the shift registers allow for counts up to 48. The sum of these two signals is then the output of adder 68, and the waveform of this output signal 70 is shown in **FIG. 11**. Detector 72 then acts to discriminate between logical 1s and logical 0s and the output signal 52 of the detector 72 is shown in the waveform illustrated in **FIG. 12**. The output of detector 72 is a rolling average that indicates a "count per bit" and, thus, the operation of the shift registers 64A and 64B, the adder 68 and the detector 72 mimics the operation of an analog low-pass filter.

[0043] As indicated above, the output of detector 72 is an over-sampled data stream and not the true received data. It therefore remains to extract the true received data from this over-sampled data stream. It is known that the data is modulated at 1 MHz, but what is not known at this point in the receive chain is where the sample clock should be set in order to extract true data. Thus, a timing recovery unit 46 (see **FIG. 3**) is used in order to align a free-running clock in the receiver with the transmitter clock in order to properly extract the data.

[0044] **FIG. 13** is a waveform diagram illustrating one example of the output signal 76 from edge detector 74. By comparing this illustration to the waveform shown in **FIG. 12**, one can see that both rising and falling transitions

are used to produce the output signal 76. **FIG. 14** illustrates the waveform of the 1 MHz clock 1680.

[0045] **FIG. 15** illustrates an example of the operation of an edge detector 74. Input signal 52 is provided as an input to a flip-flop 94, which is clocked at the 24 MHz rate. The output thereof, along with signal 52, is provided as an input to an exclusive OR (XOR) gate 96, and the resulting output signal 76 is produced.

[0046] A detailed view of a timing recovery unit 46 is shown in **FIGS. 16A** and **16B**. **FIG. 16A** is a diagram illustrating operation of an edge detector 1641 and edge shifter 1620. Edge detector 1641 receives over-sampled data signal 52 from the discriminator 40 and outputs a signal 1630 to edge shifter 1620. Edge shifter 1620 outputs a signal 1650 that may advance or delay counter 1651 one cycle, or not. Counter 1651 outputs recovered clock signal 1680 to NOT gate 1690. NOT gate 1690 drives D-flip-flop 1670 to throughput data signal 1660.

[0047] **FIG. 16B** presents a detailed view of the internal architecture of the edge detector 1641 and edge shifter 1620 shown in FIG. 16A. The 48 Mhz output 52 of discriminator 44 enters D-flip-flop 71, which is driven by a 24 Mhz clock signal 72. The effect of D-flip-flop 71 is to halve the frequency of signal 70. Thus, signal 91, outputted by D-flip-flop 71 has a 24 Mhz frequency. Signal 91 is simultaneously routed to XOR gate 73 directly and via D-flip-flop 74 to detect the rising edge of signal 91.

[0048] XOR gate 73 outputs signal 92 to AND gate 76. AND gate 76 also receives an input from comparator 93 if the variable input value to comparator 93

exceeds 20. AND gate 76 outputs a signal 85 to AND gates 77 and 82. AND gate 77 receives additional inputs from comparator 89 and from NOT gate 81. Comparator 89 receives an output from counter 88, while NOT gate 81 receives the recovered clock signal 1680. AND gate 82 receives additional input from comparator 90. AND gate 82 also receives the recovered clock signal 1680 directly.

[0049] The purpose of AND gates 77 and 82 is to determine whether the midpoint of data signal 1601 (in **FIG. 16D**) is leading or trailing the leading edge 1606 of clock signal 1602. Because data signal 1601 is sampled using the leading edge 1606 of clock signal 1602, misalignment of the leading edge 1606 of clock signal 1602 and the midpoint 1604 of data signal 1601 may cause transmission errors. For example, signal 1601 in **FIG. 16D** would be incorrectly read as a binary 11 because the period of data signal 1601 (e.g. 1 microsecond +) exceeds the period (1 microsecond) of clock signal 1602.

[0050] Thus, when AND gate 77 outputs signal 86 to have a binary value of 1, the leading edge 1606 of clock signal 1602 is too close to the falling edge 1605 of data signal 1601 (see, **FIG. 16C**). Accordingly, counter 88 is increased by one cycle to advance data signal 1601 until midpoint 1604 aligns wth leading edge 1606.

[0051] When AND gate 82 outputs signal 67 to have a binary value of 1, the leading edge 1606 of clock signal 1602 is too close to the leading edge 1603 of data signal 1601 (**FIG. 16C**). Accordingly, counter 88 is delayed by one cycle to delay data signal 1601 until midpoint 1604 of data signal 1601 aligns with the leading edge 1606 of clock signal 1602.

[0052] OR gate 78 ensures that counter 79 is reset (80) each time counter 88 is advanced or delayed. NOT gate 83 drives D-flip-flop 84 to throughput data signal 1660.

[0053] **FIG. 17** illustrates the waveform of data signal 42 for the example cited throughout this description.

[0054] Thus, a low deviation index demodulation scheme has been described. Although discussed with reference to certain illustrated embodiments, it should be remembered that the present invention should only be limited in terms of the claims that follow.